C2 C1 C0 - i/p carry for full Adder

A3 A2 A1 A0

+ B3 B2 B1 B0

Cout S3 S2 S1 S0

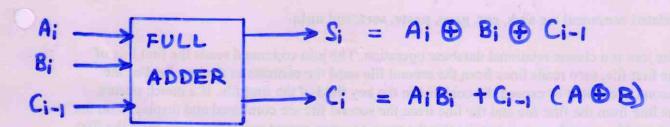
+ Cout S3 S2 S1 S0

+ Cout S3 S2 S1 S0

- result so & co is obtained after the delay of tp
- result s, & c, after the delay of 2tp.
- result S2 & C2 after the dely of 3tp.
- result Sz & Cout after the delay of 4tp.

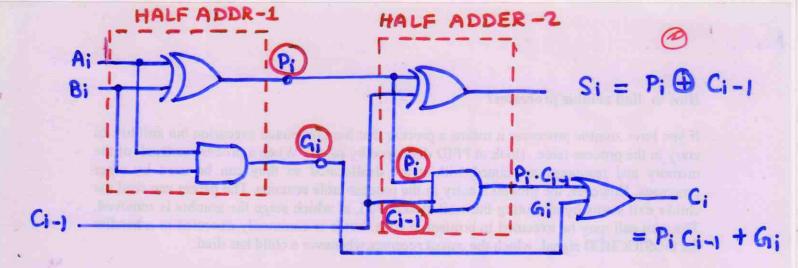
Hence, for N-Bit Parrallel Adder, total delay time is Ntp.

> Parallel Adder has larger propogation delay & hence low speed of operation. this limitation is overcomed in Carry Look Ahead Adder.



Carry Propagate function Pi = Ai
Bi : associated with propagation of Carry from Ci-1 to Ci
Carry Generate function Gi = Ai Bi : its value doesn't depend on i/p carry (Ci-1)

Hence, $Si = Pi \oplus Ci-1$ Ci = Gi + Pi Ci-1



Carry olp from first full Adder,

carry of from second,

$$C_1 = G_1 + P_0 C_0 = G_1 + P_1 (G_0 + P_0 C_{-1})$$

= $G_1 + G_0 P_1 + P_0 P_1 C_{-1}$

Carry ofp from third,

= G2 + G, P2 + G0 P, P2 + P0P, P2 C-1

Carry of from four,

C3 = G3 + G2P3 + G1 P2P3 + G0P1P2 P3 +

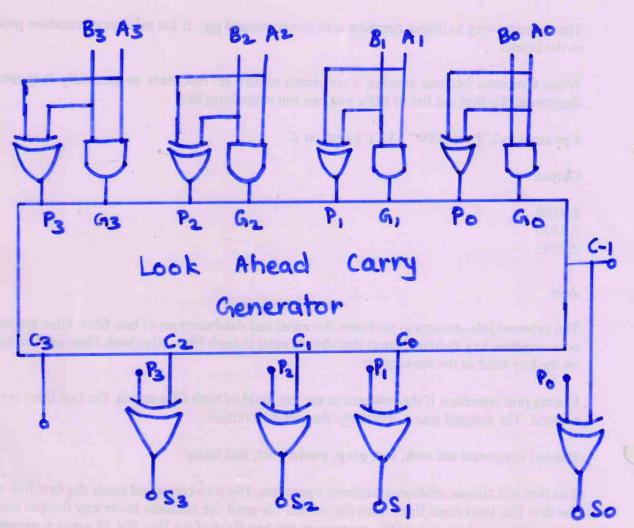
Po P1 P2 P3 C-1

Expression for carry old of each stage in 4-bit parallel Adder.

Variables are Go, G1, G2, G3, Po, P1, P2, P3, C-1

- G variables are generated from A and B i/ps using AND
- P variables are generated from A and B ilps using Ex-OR
- If G. P and Gy are at a time available, then it is possible to produce carry of Co, C,, Cz, C3

- The advantage of generating carry of p using this method is that propogation delay of only two gates will be involved.
- these carry outputs are connected to the carry inputs of succeeding stage. This elliminates problem.



LOOK AHEAD CARRY GENERATOR FOR 4-BIT ADDER.

where, $S_i = P_i \oplus C_{i-1}$ $P_i = A_i \oplus B_i$ $G_i = A_i \cdot B_i$

IC 74182 is Look Ahead Carry Generator.